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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,908	08/18/2003	Cher Khng Victor Tan	2269-5163.1US (01-0910.01	3189

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EXAMINER	
ROMAN, ANGEL	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/642,908	TAN ET AL.	
	Examiner	Art Unit	
	Angel Roman	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-29 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-29 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 18 August 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/120,169.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 09/11/03 ,01/09/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Specie III, figure 8 in the reply filed on 06/10/04 is acknowledged.

Information Disclosure Statement

2. The information disclosure statements (IDS) submitted on 09/11/03 and 01/09/04 are being considered by the examiner, however the Miller and Webpage documents were not present in the application and were not considered by the examiner, resubmit references for consideration.

Response to Amendment

3. The preliminary amendment filed 11/07/04 has been entered in the application.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-4, 9-11 and 15-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Steffen U.S. Patent 5,041,395.

Steffen discloses a method for forming a semiconductor device assembly by designing a solder mask for use on a carrier substrate, comprising; providing a carrier substrate including at least one die-attach location 12 and at least one terminal 14 adjacent to the at least one die-attach location 12; and providing a solder mask on the carrier substrate, the solder mask including at least one device-securing region positioned over at least a portion of the at least one die-attach location 12, at least one recessed area 16 adjacent to the at least one device-securing region, and at least one raised dam 20 adjacent to the at least one recessed area 16, opposite from the at least one device-securing region 12, the at least one dam 20 contacting at least a portion of a peripheral edge of the at least one terminal 14, the dam 20 having a height at least as great as or greater than the device securing region (see figure 3). Steffen also discloses applying adhesive material to at least one of the at least one device-securing region of the solder mask and a bottom surface of at least one semiconductor device 26 and securing the device 26 by applying force to at least one of the device and the carrier substrate (see figure 4) to the at least one device-securing region (see column 4, lines 57-61). Providing the solder mask comprises providing a solder mask with the at least one dam 20 comprising a laterally extending portion configure to cover at least one

portion of a peripheral edge of a connection surface of the at least one terminal 14 (see figure 3). The solder mask is provided by securing a preformed solder mask to the substrate thereby providing a carrier substrate with the solder mask secured thereto (see figures 1-3).

6. Claims 1-8, 10, 12, 15-19 and 22-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Fontecha et al. U.S. Patent 6,448,507 B1.

Fontecha et al. discloses a method for forming a semiconductor device assembly, a carrier substrate and designing a solder mask 14, comprising; providing a carrier substrate 10 including at least one die-attach location and at least one terminal 13 adjacent to the at least one die-attach location; and providing a solder mask 14 on the carrier substrate, the solder mask including at least one device-securing region positioned over at least a portion of the at least one die-attach location, at least one recessed area 15 adjacent to the at least one device-securing region and between at least a portion of a periphery of the at least one device-securing region and at least one of a plurality of raised dams and substantially laterally surrounding one die attach location and adjacent to only a portion of the die attach location (see figure 1), the raised dams contacting at least a portion of a peripheral edge of the at least one terminal 13 and having a height at least as great as the device-securing region and less than an elevation of an active surface of a semiconductor device to be positioned on the at least one device-securing region (see figure 2). Fontecha et al. also discloses applying adhesive material 12 to at least one of the device-securing region of the solder

mask and a bottom surface of at least one semiconductor device 11 secured to the at least one device-securing region (see column 3, lines 40-62). 4. The device 11 is secured by applying force to at least one of the at least one semiconductor device 11 and the carrier substrate 10 thereby forcing the adhesive material 12 to spread between a bottom surface of the at least one semiconductor device 11 and the at least one device-securing region causing excess adhesive material 12 to flow laterally beyond at least one of a peripheral edge of the at least one semiconductor device 11 and a periphery of the at least one device-securing region wherein the excess adhesive material is received within the at least one recessed area 15 and wherein the dam prevents the excess adhesive material 12 from contaminating a connection surface of the at least one terminal 13 (see figure 2). The solder mask is formed on the carrier substrate 10 thereby providing a carrier substrate with a solder mask secured thereto (see column 3, lines 40-62).

7. Claims 23 and 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Bhatt et al. U.S. Patent 6,426,565 B1.

Bhatt et al. discloses a method for designing a carrier substrate, comprising; configuring a substantially planar substrate 12 to include at least one die-attach location, configuring at least one terminal 32 adjacent to the at least one die-attach location and to protrude a sufficient distance from the substantially planar substrate 12 to prevent excess adhesive material forced from between a semiconductor device 34 and the at least one die-attach location from contaminating a connection surface of the

at least one terminal 32, wherein configuring the one terminal comprises configuring the at least one terminal to have a height that is, at most, substantially the same as an elevation at which a top surface of the semiconductor device 34 will be located upon securing the semiconductor device 34 relative to the substantially planar substrate 12 (see figure 1).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fontecha et al. U.S. Patent 6,448,507 B1.

Fontecha et al. s applied as above but lacks anticipation on forming the solder mask 14 using a stereolithography process or disclosing a plurality of at least partially superimposed, contiguous, mutually adhered material layers used to formed the solder mask. Fontecha et al. clearly suggest using conventional solder mask material such as a combination of epoxy-based resins, e.g., superimposed, contiguous, mutually adhered material layers (see column 6, lines 25-30), therefore it would have been obvious to one having ordinary skills in the art at the time the invention was made to form the solder mask 14 using a stereolithography process with a combination of at least partially superimposed, contiguous, mutually adhered epoxy-based resins in order to form a desire recess 15 in the solder mask 14.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ujiie et al., Hsu et al., Terui et al., Wu et al., Farquhar et al., Fusaro et al., Fujisawa et al., Shim et al., Tsuruzono, Newman, Humphrey et al. and

Hoffman et al. disclosed methods of preventing contamination of substrate contacts with an adhesive used to attach a semiconductor device to the substrate.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel Roman whose telephone number is (571) 272-1681. The examiner can normally be reached on Monday-Friday 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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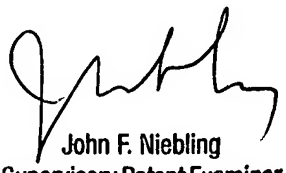
August 28, 2004



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